REMARKS/ARGUMENTS

Claims 1-20 are pending in this application. The Office Action, dated December 17, 2004: rejected claim 2 under 35 USC § 112, second paragraph, rejected to claim 1-3, 5-8 and 12-20 under 35 USC § 102(b), and objected to claims 4 and 9-11 as based on a rejected base claim but are otherwise allowable, and accepted the drawings filed on December 15, 2003. Applicant thanks the Examiner for the review and indication of allowable subject matter for claims 4 and 9-11. Claims 1 and 13 are amended, not to overcome any basis of rejection, but merely to correct for a minor infelicity. The objections and rejections are believed to be overcome for the reasons stated below. No new matter is added.

Drawings

The office action stated that the drawings filed on December 15, 2003 are accepted without any objections. While Applicant appreciates such consideration, replacement sheets were submitted to the USPTO on September 23, 2004 and such notice has been made in the USPTO PAIR system. Applicant's respectfully request that the formal drawing submissions made on September 23, 2004 be considered and entered in the record. Applicant kindly request the Examiner contact Applicant's counsel in the event that the drawings are misplaced and require resubmission.

Rejection of Claim 2 under 35 USC § 112, second paragraph

Claim 2 is rejected under 35 USC § 112, second paragraph, for failing to point out and distinctly claim the subject matter which Applicant regards as the invention. In particular, the office action notes that the claim element "a first transistor" in claim 2 is improper since it has

already been recited in claim 1. Applicant respectfully disagrees. claim 1 recites " a first transistor **circuit**", while claim 2 recites "a first transistor". These elements do not overlap and are distinctly different. It is respectfully requested that the rejection under 35 USC § 112, second paragraph be withdrawn and notice to that effect is requested.

Rejection of Claims 1-3, 5-8, and 12-20 under 35 USC § 102(b)

Claims 1-3, 5-8, and 12-20 are rejected under 35 USC § 102(b) as being anticipated by D'Angelo (US Patent No. 6,166,530). The office action states:

> "With respect to claim 103, 5-8 and 12-16, D'Angelo discloses, in Fig. 5, a circuit comprising: "a power device (102 and 114)"; "a load(104)"; "a current sense circuit (148-152)"; "a first transistor (110)"; "a second transistor (one or more of 128-136)", a comparator (140-146)"; and "a level shifter (154)", all connected and operating similarly as recited by Applicant.
>
> With respect to claim 17-20, clearly the above circuit to D'Angelo will provide the recited method."

The office action is silent as to any other basis of rejection. Applicant would like to point out that claims 1 - 12 comprise a first set of apparatus claims, claims 13-16 comprise a second set of apparatus claims, and claims 17 - 20 comprise a set of method claims. Each of these claim sets is entitled to a complete analysis on the merits. Applicant respectfully requests that the claims be fully evaluated, and that an action on the merits be provided with sufficient guidance so that the Applicant can fully appreciate any basis of rejection. As a courtesy to the Examiner, the Applicant has made every effort to evaluate the cited references and provide guidance to appreciate the distinctions between those references and the claimed invention.

Applicant's have taken the liberty to review the D'Angelo reference in great detail, noting the differences between the Applicant's claimed invention and that which is taught in by the figures, most notably FIG. 5. Although the Applicant has noted individual differences between the claimed invention and the D'Angelo reference, Applicant believes that the claimed invention must be considered as a whole. In consideration of these and other factors, Applicant believes that at least the following claim elements (in pertinent part) from Applicant's claim 1 are not found in the cited prior art references:

> "a current sense circuit that is arranged ... **such that the operating current of the apparatus does not dramatically rise** when a short-circuit condition is present across the load circuit;
> a first transistor circuit ... **arranged to deactivate the power device** when a short-circuit detection signal is asserted;
> a second transistor circuit ... **arranged to couple a small current to the load circuit** when the short-circuit detection signal is asserted **such that** the apparatus automatically **returns to a normal operating mode** when the short-circuit condition is removed ...; and
> **a comparator circuit** ... **arranged to assert the short-circuit detection signal** ..."

Element 114 is not a power device as stated in the office action, and is instead a difference amplifier circuit (see col. 5, lines 33 - 38, and lines 56-58).

Transistors 148 - 152 are not a current sense circuit as stated in the office action, and instead these transistors are diode connected devices that operate as a voltage divider circuit (see col. 6, lines 32-39).

Although element 110 is in fact a first transistor, the structural limitations of "a first transistor circuit" from Applicant's claim 1 requires that the first transistor **circuit** be arranged in relation to the remaining claim elements. Applicant's claim 1 does not call merely for a

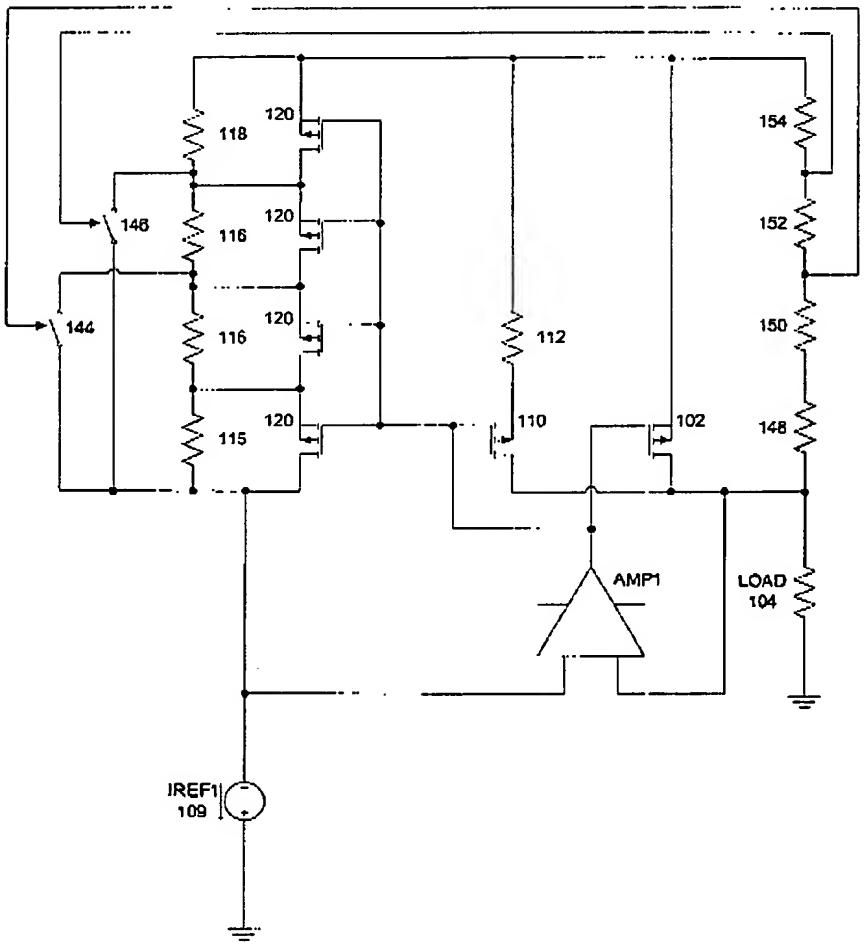
transistor, and instead calls for "a first transistor circuit that is arranged to deactivate the power device when a short-circuit detection signal is asserted". These structural requirements are simply not met by transistor 110 which instead just tracks the current in transistor 102 (see col. 5, lines 13-18).

Elements 128-136 are actually intermediary nodes and not transistors as suggested in the office action. Applicant believes the office action is referring to transistors 120, which are coupled to nodes 128 - 136 and will respond accordingly. Although transistor(s) 120 can generically be referred to as a second transistor(s), the structural limitations of "a second transistor circuit" from Applicant's claim 1 requires that the second transistor **circuit** be arranged in relation to the remaining claim elements. Applicant's claim 1 does not call merely for a transistor, and instead calls for "a second transistor circuit ... **arranged to couple a small current to the load circuit** when the short-circuit detection signal is asserted **such that** the apparatus automatically **returns to a normal operating mode** when the short-circuit condition is removed." These structural relationships are simply not met by transistors 120. Instead, transistors 120 are taught as part of a current mirror circuit (see col. 5, lines 27 - 30) that can be selectively disabled by transistors 140 - 146, which operate as bypass switches (see col. 6, lines 40 - 48).

Element 154 is not a level shifter as stated in the office action. Instead, elements 154 is arranged as a diode connected transistor that that operates as part of the voltage divider circuit (see col. 6, lines 32-39). Moreover, applicant's claims 7, 8, 9 and 11 do not merely require any

level shifting function, but instead requires a structural relationship with other claim elements such that level shifting functions are provided to an input of a comparator (see e.g., claim 7).

A simplified diagram is provided to assist in explaining the circuits of FIG. 5 from the D'Angelo reference.



Transistors 144 and 146 are arranged to operate as bypass switches as illustrated above. Transistors 148 - 154 are arranged to operate as a voltage divider, so they are represented as

series resistors for simplicity, where the tap point in the voltage divider controls the actuation of the bypass switches. Transistors 120 are commonly biased with transistors 110 and 102, and operate as part of a current mirror. The amplifier circuit (AMP1) linearly controls the gate voltage associated with transistors 102, 110, and 120 to provide a limit to the amount of output current that is provided to the load.

With respect to claim 13, Applicant is not certain how the office action has applied the references since no guidance is provided. Applicant believes that claim 13, taken as a whole is novel, non-obvious, and contains at least the following features (in pertinent part) that are not found in the prior art of record:

> "a current sense means ... arranged ... such that there is approximately no DC current in the apparatus **when a short-circuit condition is present** across the load circuit;
>
> a disabling means ... **arranged to disabled the power device** when a short-circuit detection signal is asserted;
>
> a recovery current means ... arranged to provide a small current (I) ... such that the apparatus **automatically returns to a normal operating mode when the short-circuit condition is removed** from the load circuit;
>
> a comparator means ... arranged to assert the short-circuit detection signal ...; and
>
> a minimum over-drive means ... arranged to **maintain at least one input signal to the comparator means at a minimum over-drive level** (Vmin_OD) when the short circuit condition is present."

With respect to claim 17, Applicant is not certain how the office action has applied the references since no guidance is provided. Applicant believes that claim 17, taken as a whole is novel, non-obvious, and contains at least the following features (in pertinent part) that are not found in the prior art of record:

"asserting a short-circuit detection signal when the sensed output voltage is less than the sense signal;

disabling the power device when the short-circuit detection signal is asserted;

enabling a current source when the short-circuit detection signal is asserted, wherein the current source is coupled to the load circuit;

increasing the output voltage across the load with the current source when the short-circuit condition is removed from the load circuit;

detecting when the short circuit condition is removed from the load circuit; and

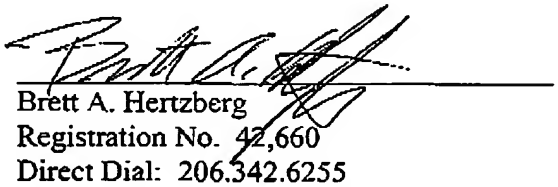
enabling the power device when the short-circuit condition is detected as removed from the load circuit"

Since not all of the claim elements are found in any one of the cited prior art references, it is believed that the rejection of the claims is traversed. Claims 1-20 are proposed to be allowable for the reasons discussed above, and a notice to that effect is requested.

In view of the foregoing amendments and remarks, all pending claims are believed to be allowable and the application is in condition for allowance. Therefore, a Notice of Allowance is respectfully requested. Should the Examiner have any further issues regarding this application, the Examiner is requested to contact the undersigned attorney for the applicant at the telephone number provided below.

Respectfully submitted,

MERCHANT & GOULD P.C.



Brett A. Hertzberg
Registration No. 42,660
Direct Dial: 206.342.6255

MERCHANT & GOULD P.C.
P. O. Box 2903
Minneapolis, Minnesota 55402-0903
206.342.6200
BAH/ab

23552
PATENT TRADEMARK OFFICE